

EXHIBIT H



US007383453B2

(12) **United States Patent**
Youngs

(10) **Patent No.:** **US 7,383,453 B2**

(45) **Date of Patent:** ***Jun. 3, 2008**

(54) **CONSERVING POWER BY REDUCING VOLTAGE SUPPLIED TO AN INSTRUCTION-PROCESSING PORTION OF A PROCESSOR**

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(*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 55 days.

This patent is subject to a terminal disclaimer.

(21) **Appl. No.:** **11/213,215**

(22) **Filed:** **Aug. 25, 2005**

(65) **Prior Publication Data**
US 2005/0283628 A1 Dec. 22, 2005

Related U.S. Application Data

(63) Continuation of application No. 11/103,911, filed on Apr. 11, 2005, now Pat. No. 6,973,585, which is a continuation of application No. 10/135,116, filed on Apr. 29, 2002, now Pat. No. 6,920,574.

(51) **Int. Cl.**
G06F 1/00 (2006.01)
G06F 1/26 (2006.01)

(52) **U.S. Cl.** **713/300; 713/320; 713/324**

(58) **Field of Classification Search** 713/300
See application file for complete search history.

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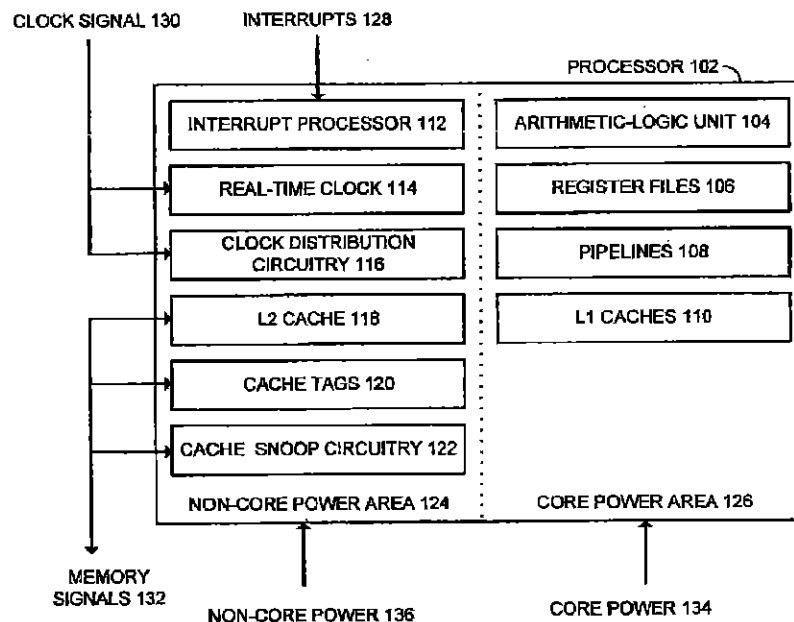
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(57) **ABSTRACT**

One embodiment of the present invention provides a system that facilitates reducing static power consumption of a processor. During operation, the system receives a signal indicating that instruction execution within the processor is to be temporarily halted. In response to this signal, the system halts an instruction-processing portion of the processor, and reduces the voltage supplied to the instruction-processing portion of the processor. Full voltage is maintained to a remaining portion of the processor, so that the remaining portion of the processor can continue to operate while the instruction-processing portion of the processor is in reduced power mode.

21 Claims, 3 Drawing Sheets



U.S. Patent

Jun. 3, 2008

Sheet 1 of 3

US 7,383,453 B2

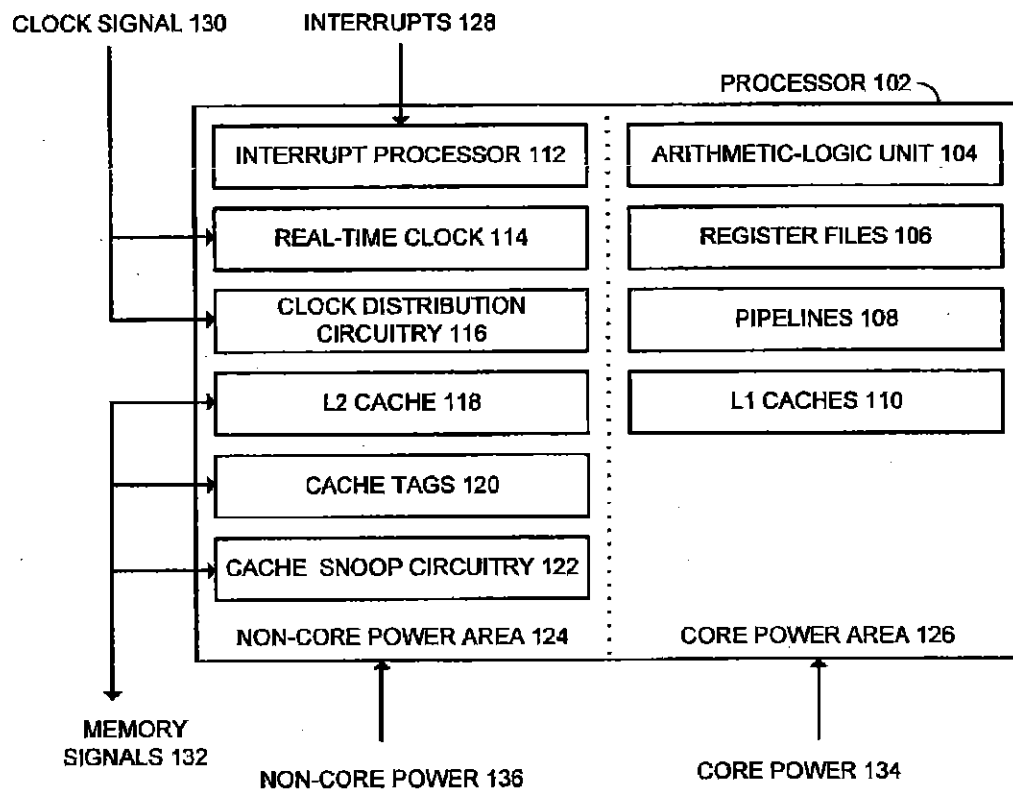


FIG. 1A

U.S. Patent

Jun. 3, 2008

Sheet 2 of 3

US 7,383,453 B2

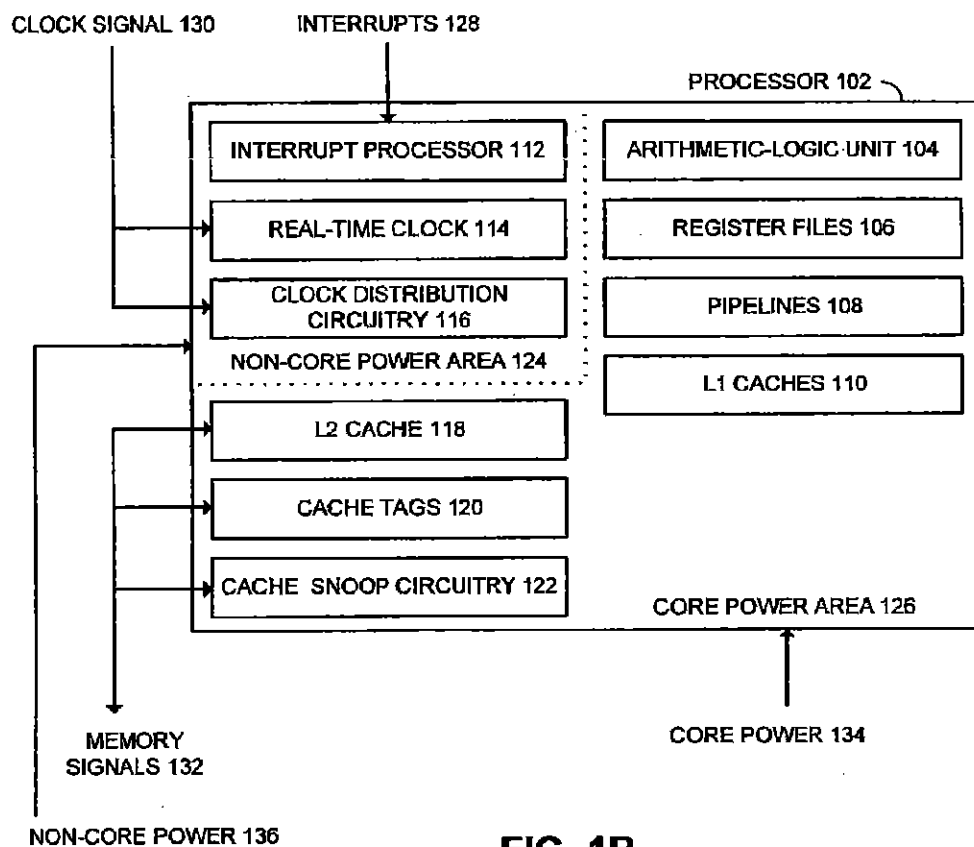


FIG. 1B

U.S. Patent

Jun. 3, 2008

Sheet 3 of 3

US 7,383,453 B2

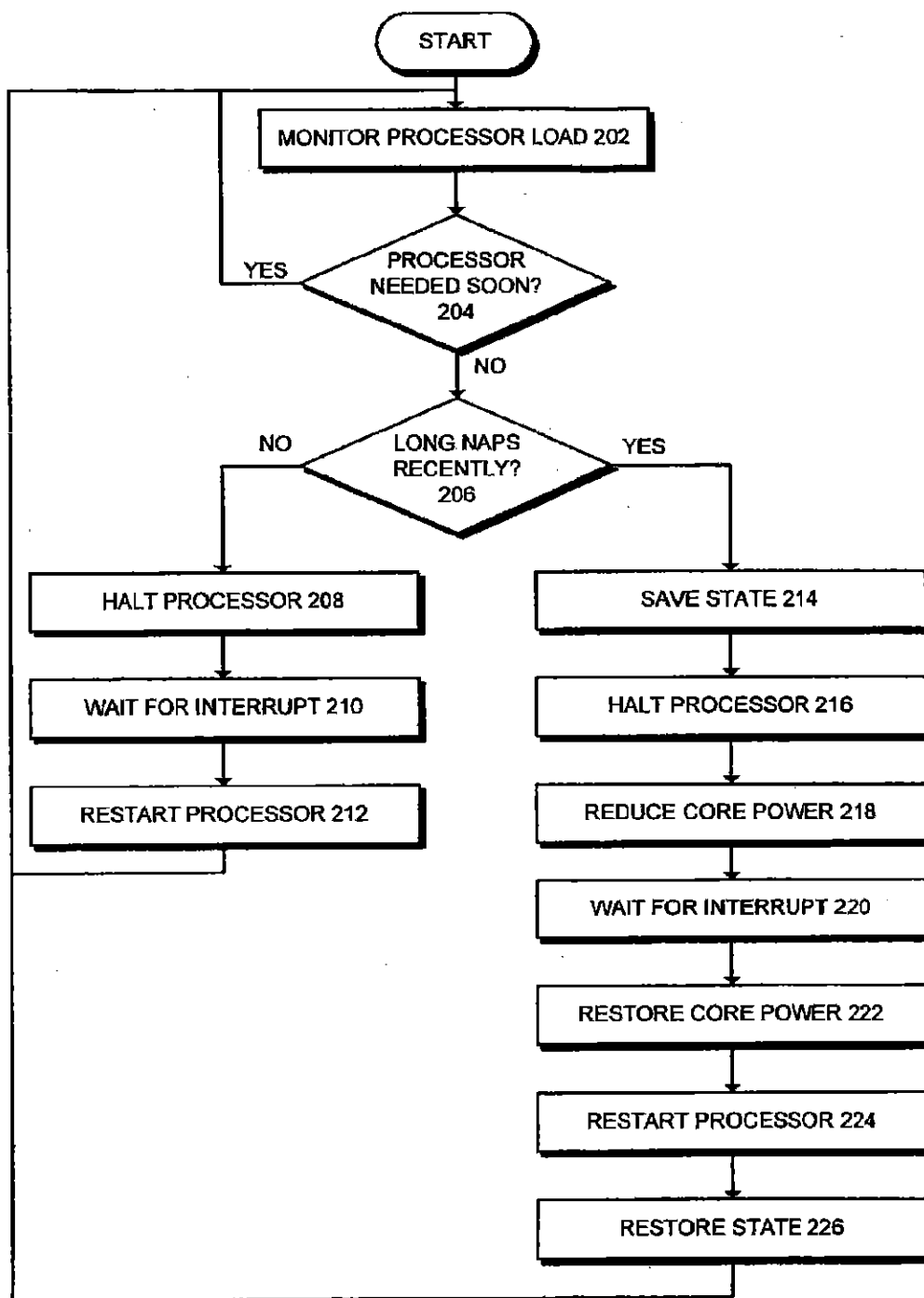


FIG. 2

US 7,383,453 B2

1

CONSERVING POWER BY REDUCING VOLTAGE SUPPLIED TO AN INSTRUCTION-PROCESSING PORTION OF A PROCESSOR

RELATED APPLICATION

This application is a continuation of U.S. patent application Ser. No. 11/103,911, filed 11 Apr. 2005 now U.S. Pat. No. 6,973,585. This application hereby claims priority under 35 U.S.C. §120 to the above-listed application. Note that pending U.S. patent application Ser. No. 11/103,911 is itself a continuation of U.S. patent application Ser. No. 10/135,116, filed 29 Apr. 2002 now U.S. Pat. No. 6,920,574.

BACKGROUND

1. Field of the Invention

The present invention relates to techniques for conserving power usage in computer systems. More specifically, the present invention relates to a method and an apparatus for reducing power consumption in a processor by reducing voltage supplied to an instruction-processing portion of the processor, while maintaining voltage to other portions of the processor.

2. Related Art

Dramatic advances in integrated circuit technology have led to corresponding increases in processor clock speeds. Unfortunately, these increases in processor clock speeds have been accompanied by increased power consumption. Increased power consumption is undesirable, particularly in battery-operated devices such as laptop computers, for which there exists a limited supply of power. Any increase in power consumption decreases the battery life of the computing device.

Modern processors are typically fabricated using Complementary Metal Oxide Semiconductor (CMOS) circuits. CMOS circuits typically consume more power while the circuits are switching, and less power while the circuits are idle. Designers have taken advantage of this fact by reducing the frequency of (or halting) clock signals to certain portions of a processor when the processor is idle. Note that some portions of the processor must remain active, however. For example, a cache memory with its associated snoop circuitry will typically remain active as well as interrupt circuitry and real-time clock circuitry.

Although reducing the frequency of (or halting) a system clock signal can reduce the dynamic power consumption of a processor, static power consumption is not significantly affected. This static power consumption is primarily caused by leakage currents through the CMOS devices. As integration densities of integrated circuits continue to increase, circuit devices are becoming progressively smaller. This tends to increase leakage currents, and thereby increases static power consumption. This increased static power consumption results in reduced battery life, and increases cooling system requirements for battery operated computing devices.

What is needed is a method and an apparatus that reduces static power consumption for a processor in a battery operated computing device.

SUMMARY

One embodiment of the present invention provides a system that facilitates reducing static power consumption of a processor. During operation, the system receives a signal

2

indicating that instruction execution within the processor is to be temporarily halted. In response to this signal, the system halts an instruction-processing portion of the processor, and reduces the voltage supplied to the instruction-processing portion of the processor. Full voltage is maintained to a remaining portion of the processor, so that the remaining portion of the processor can continue to operate while the instruction-processing portion of the processor is in reduced power mode.

In one embodiment of the present invention, reducing the voltage supplied to the instruction-processing portion of the processor involves reducing the voltage to a minimum value that maintains state information within the instruction-processing portion of the processor.

In one embodiment of the present invention, reducing the voltage supplied to the instruction-processing portion of the processor involves reducing the voltage to zero.

In one embodiment of the present invention, the system saves state information from the instruction-processing portion of the processor prior to reducing the voltage supplied to the instruction-processing portion of the processor. This state information can either be saved in the remaining portion of the processor or to the main memory of the computer system.

In one embodiment of the present invention, upon receiving a wakeup signal, the system: restores full voltage to the instruction-processing portion of the processor; restores state information to the instruction-processing portion of the processor; and resumes processing of computer instructions.

In one embodiment of the present invention, maintaining full voltage to the remaining portion of the processor involves maintaining full voltage to a snoop-logic portion of the processor, so that the processor can continue to perform cache snooping operations while the instruction-processing portion of the processor is in the reduced power mode.

In one embodiment of the present invention, the system also reduces the voltage to a cache memory portion of the processor. In this embodiment, the system writes cache memory data to main memory prior to reducing the voltage.

In one embodiment of the present invention, the remaining portion of the processor includes a control portion of the processor containing interrupt circuitry and clock circuitry.

In one embodiment of the present invention, the remaining portion of the processor includes a cache memory portion of the processor.

BRIEF DESCRIPTION OF THE FIGURES

FIG. 1A illustrates different power areas within processor 102 in accordance with an embodiment of the present invention.

FIG. 1B illustrates alternate power areas within processor 102 in accordance with an embodiment of the present invention.

FIG. 2 is a flowchart illustrating the process of monitoring processor load and switching to power saving modes in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

The following description is presented to enable any person skilled in the art to make and use the invention, and is provided in the context of a particular application and its requirements. Various modifications to the disclosed embodiments will be readily apparent to those skilled in the art, and the general principles defined herein may be applied to other embodiments and applications without departing

US 7,383,453 B2

3

from the spirit and scope of the present invention. Thus, the present invention is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features disclosed herein.

Processor 102

FIG. 1A illustrates different power areas within processor 102 in accordance with an embodiment of the present invention. Processor 102 is divided into a core power area 126, and a non-core power area 124. Core power area 126 includes the instruction-processing portion of processor 102. Specifically, core power area 126 includes arithmetic-logic unit 104, register files 106, pipelines 108, and possibly level one (L1) caches 110. Note that L1 caches 110 can alternatively be located in non-core power area 124.

Arithmetic-logic unit 104 provides computational and logical operations for processor 102. Register files 106 provide source operands, intermediate storage, and destination locations for instructions being executed by arithmetic-logic unit 104. Pipelines 108 provides a steady stream of instructions to arithmetic-logic unit 104. Instructions in pipelines 108 are decoded in transit. Therefore, pipelines 108 may contain instructions in various stages of decoding and execution. L1 caches 110 include data caches and instruction caches for arithmetic-logic unit 104. L1 caches 110 are comprised of very high-speed memory to provide fast access for instructions and data. In one embodiment of the present invention, L1 caches 110 includes a write-through data cache.

Non-core power area 124 comprises the remaining portion of processor 102 and includes interrupt processor 112, real-time clock 114, clock distribution circuitry 116, level two (L2) caches 118, cache tags 120, and cache snoop circuitry 122. In general, non-core power area 124 includes portions of processor 102 that are not directly involved in processing instructions, and that need to operate while instruction processing is halted.

Interrupt processor 112 monitors interrupts 128 and periodically interrupts the execution of applications to provide services to external devices requiring immediate attention. Interrupt processor 112 can also provide a wake-up signal to core power area 126 as described below. Real-time clock 114 provides time-of-day services to processor 102. Typically, real-time clock 114 is set upon startup from a battery operated real-time clock in the computer and thereafter provides time to the system. Clock distribution circuitry 116 provides clock signals for processor 102. Distribution of these clock signals can be switched off or reduced for various parts of processor 102. For example, clock distribution to core power area 126 can be stopped while the clock signals to non-core power area 124 continue. The acts of starting and stopping of these clock signals are known in the art and will not be described further. Real-time clock 114 and clock distribution circuitry 116 receive clock signal 130 from the computer system. Clock signal 130 is the master clock signal for the system.

L2 cache 118 provides a second level cache for processor 102. Typically, an L2 cache is larger and slower than an L1 cache, but still provides faster access to instructions and data than can be provided by main memory. Cache tags 120 provide an index into data stored in L2 cache 118. Cache snoop circuitry 122 invalidates cache lines base primarily on other processors accessing their own cache lines, or I/O devices doing memory transfers, even when instruction processing has been halted. L2 cache 118, cache tags 120, and cache snoop circuitry 122 communicate with the computer system through memory signals 132.

4

Non-core power area 124 receives non-core power 136 and core power area 126 receives core power 134. The voltage applied for non-core power 136 remains at a voltage that allows circuitry within non-core power area 124 to remain fully active at all times. In contrast, non-core power 136 may provide different voltages to non-core power area 124 based upon the operating mode of processor 102. For example, if processor 102 is a laptop attached to external electrical power, the voltage provided to non-core power 136 (and to core power 134 during instruction processing) may be higher than the minimum voltage, thus providing faster execution of programs.

The voltage applied to core power 134 remains sufficiently high during instruction processing so that core power area 126 remains fully active. However, when processor 102 receives a signal that processing can be suspended, the voltage supplied by core power 134 can be reduced.

In one embodiment of the present invention, the voltage in core power 134 is reduced to the minimum value that will maintain state information within core power area 126, but this voltage is not sufficient to allow processing to continue. In another embodiment of the present invention, the voltage at core power 134 is reduced to zero. In this embodiment, the state of core power area 126 is first saved before the voltage is reduced to zero. This state can be saved in a dedicated portion of L2 cache 118, in main memory, or in another dedicated storage area. Upon receiving an interrupt or other signal indicating that processing is to resume, the voltage in core power 134 is restored to a normal level, saved state is restored, and processing is restarted.

FIG. 1B illustrates an alternative partitioning of power areas within processor 102 in accordance with an embodiment of the present invention. As shown in FIG. 1B, L2 cache 118, cache tags 120, and cache snoop circuitry 122 are included in core power area 126 rather than in non-core power area 124. In this embodiment, the voltage supplied as core power 134 is reduced or set to zero as described above, however, the cache circuitry within processor 102 is also put into the reduced power mode. Prior to reducing the voltage supplied to core power area 126, data stored in L2 cache 118 is flushed to main memory. Additionally, if the voltage at core power 134 is reduced to zero, the state of processor 102 is first saved in main memory.

Monitoring and Switching

FIG. 2 is a flowchart illustrating the process of monitoring processor load and switching to power saving modes in accordance with an embodiment of the present invention. The system starts by monitoring the processor load (step 202). Next, the system determines if the processor will be needed soon (step 204). This determination is made based on the current execution pattern and the cost of entering and recovering from nap mode. This cost, calculated in power usage, must be less than the power wasted by not going into nap mode. If the processor will be needed soon at step 204, the process returns to step 202 to continue monitoring the processor load.

If the processor will not be needed soon at step 204, the system determines if the processor has been taking long naps recently (step 206). If not, the system enters a normal nap mode, which involves halting the processor without reducing any voltages (step 208). Typically, halting the processor involves removing the clock signals to the core power area of the processor. After halting the processor, the system waits for an interrupt (step 210). Upon receiving an interrupt or other signal requiring a restart, the system restarts instruc-

US 7,383,453 B2

5

tion processing (step 212). After restarting instruction processing, the process returns to step 202 to continue monitoring the processor load.

If the processor has recently been taking long naps at step 206, the system enters a deep nap mode, which involves saving the state information from the core power area (step 214), halting the processor (step 216), and then reducing the voltage supplied to the core power area (step 218). After reducing the voltage, the system waits for an interrupt (step 220).

Upon receiving the interrupt or other signal requiring a restart, the system restores the voltage to the core power area (step 222). Next, the modules within the core power area are restarted (step 224). The system then restores the state information that was saved at step 214 (step 226). After the processor has been restarted, the process returns to step 202 to continue monitoring the processor load. Note that the above description applies when the processor is used to save and restore the state information. In cases where dedicated hardware saves and restores the state information, steps 214 and 216, and steps 224 and 226 can be reversed. Note also that if the voltage supplied to the core power area 126 is reduced but maintained at a level where modules in the core power do not lose state information, steps 216 and 224 are not required.

The foregoing descriptions of embodiments of the present invention have been presented for purposes of illustration and description only. They are not intended to be exhaustive or to limit the present invention to the forms disclosed. Accordingly, many modifications and variations will be apparent to practitioners skilled in the art. Additionally, the above disclosure is not intended to limit the present invention. The scope of the present invention is defined by the appended claims.

What is claimed is:

1. An instruction-processing system with minimal static power leakage, the instruction-processing system comprising:

a core with instruction-processing circuitry;

an area coupled to the core;

a core voltage provided to the core; and

an area voltage provided to the area;

wherein in a normal operation mode:

a clock signal to the core is active;

the core voltage is a first value;

the core is active;

the area voltage is a second value; and

the area is active;

wherein in a first power-saving mode that is exited upon receipt of an interrupt signal:

the clock signal to the core is inactive;

the core voltage is equal to or greater than the first value; and

the area voltage is equal to or greater than the second value;

wherein in a second power-saving mode that can be exited upon receipt of a signal that is not an interrupt signal:

the clock signal to the core is inactive;

the core voltage is less than the first value; and

the area voltage is equal to or greater than the second value.

2. The instruction-processing system of claim 1, wherein the first power-saving mode can be exited upon receipt of a signal that is not an interrupt signal.

3. The instruction-processing system of claim 1, wherein the area comprises a cache.

6

4. The instruction-processing system of claim 3, wherein the area further comprises cache tags.

5. The instruction-processing system of claim 1, wherein prior to entering the second power-saving mode, the state of the core is saved to a memory.

6. The instruction-processing system of claim 1, wherein upon exiting the second power-saving mode, the state of the core is restored.

7. The instruction-processing system of claim 1, wherein in the second power-saving mode, the core voltage is at zero.

8. A method for minimizing static power leakage in an instruction-processing system, wherein the instruction-processing system comprises a core with instruction-processing circuitry, an area coupled to the core, a core voltage provided to the core, and an area voltage provided to the area, the method comprising:

entering a normal operation mode by:

providing a clock signal to the core;

providing the core with a core voltage that is equal to a first value;

providing the area with an area voltage that is equal to a second value;

entering a first power-saving mode by:

disabling the clock signal to the core;

providing the core with a core voltage that is equal to or greater than the first value; and

providing the area with an area voltage that is equal to or greater than the second value;

exiting the first power-saving mode upon receipt of an interrupt signal;

entering a second power-saving mode by:

disabling the clock signal to the core;

setting the core voltage to a value less than the first value; and

providing the area with an area voltage that is equal to or greater than the second value; and

exiting the second power-saving mode upon receipt of a signal that is not an interrupt signal.

9. The method of claim 8, further comprising exiting the first power-saving mode upon receipt of a signal that is not an interrupt signal.

10. The instruction-processing system of claim 8, wherein the area comprises a cache.

11. The method of claim 10, wherein the area further comprises cache tags.

12. The method of claim 8, further comprising saving the state of the core to a memory prior to entering the second power-saving mode.

13. The method of claim 8, further comprising restoring the state of the core upon exiting the second power-saving mode.

14. The method of claim 8, wherein in the second power-saving mode, setting the core voltage to the value less than the first value comprises setting the core voltage to zero.

15. A computer-readable medium containing data representing an instruction-processing system with minimal static power leakage, the instruction-processing system comprising:

a core with instruction-processing circuitry;

an area coupled to the core;

a core voltage provided to the core; and

an area voltage provided to the area;

wherein in a normal operation mode:

a clock signal to the core is active;

the core voltage is a first value;

the core is active;

US 7,383,453 B2

7

the area voltage is a second value; and
the area is active;
wherein in a first power-saving mode that is exited upon
receipt of an interrupt signal:
the clock signal to the core is inactive;
the core voltage is equal to or greater than the first
value; and
the area voltage is equal to or greater than the second
value;
wherein in a second power-saving mode that can be exited 10
upon receipt of a signal that is not an interrupt signal:
the clock signal to the core is inactive;
the core voltage is less than the first value; and
the area voltage is equal to or greater than the second
value.
15
16. The computer-readable medium of claim 15, wherein
the first power-saving mode can be exited upon receipt of a
signal that is not an interrupt signal.

8

17. The computer-readable medium of claim 15, wherein
the area comprises a cache.
18. The computer-readable medium of claim 17, wherein
the area further comprises cache tags.
19. The computer-readable medium of claim 15, wherein
prior to entering the second power-saving mode, the state of
the core is saved to a memory.
20. The computer-readable medium of claim 15, wherein
upon exiting the second power-saving mode, the state of the
core is restored.
21. The computer-readable medium of claim 15,
wherein in the second power-saving mode, the core voltage
is at zero.

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